



(19)

Europäisches Patentamt  
Europäische Patent Office  
Office Européen des brevets



(11)

EP 0 810 638 A2

(12)

## EUROPEAN PATENT APPLICATION

(43) Date of publication:  
03.12.1997 Bulletin 1997/49

(51) Int Cl.<sup>6</sup>: H01L 21/20, H01L 21/316

(21) Application number: 97303455.6

(22) Date of filing: 21.05.1997

(84) Designated Contracting States:  
DE FR GB

• Mei, Ping  
Palo Alto, California 94306 (US)

(30) Priority: 31.05.1996 US 656460

• Ready, Steve  
Santa Cruz, California 95060 (US)  
• Johnson, Richard I.  
Menlo Park, California 94025 (US)  
• Anderson, Greg B.  
Woodside, California 94062 (US)

(71) Applicant: XEROX CORPORATION  
Rochester New York 14644 (US)

(74) Representative: Pike, Christopher Gerard et al  
Rank Xerox Ltd.,  
Patent Department,  
Parkway  
Marlow, Buckinghamshire SL7 1YL (GB)

(72) Inventors:

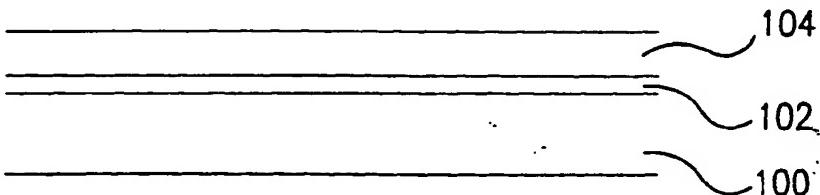
- Fork, David K.  
Palo Alto, California 94306 (US)
- Boyce, James B.  
Los Altos, California 94024 (US)

### (54) Buffered substrate for semiconductor devices

(57) The invention provides a buffered substrate that includes a substrate, a buffer layer and a silicon layer. The buffer layer is disposed between the substrate

and the silicon layer. The buffer layer has a melting point higher than a melting point of the substrate. A polycrystalline silicon layer is formed by crystallizing the silicon layer using a laser beam.

FIG.2C



## D scription

This invention relates to a structure and method for forming polycrystalline layers having uniform and small polycrystalline grain sizes.

As feature sizes of such devices as thin film transistors (TFTs) decrease with increasing device densities for such products as displays and scanners, the sizes of polycrystalline silicon grains and grain size variations become increasingly important factors in polycrystalline silicon device characteristics. In particular, as TFT feature dimensions become smaller, smaller grains are required to obtain a statistically significant number of grains within channel regions of TFTs to assure uniform device characteristics for TFTs formed in the polycrystalline silicon layer. If grain sizes are large relative to TFT feature dimensions and grain size variation is also large, TFT characteristics may vary greatly depending on the number of grain boundaries that are included in the channel regions, for example.

Conventional techniques such as laser crystallization for forming polycrystalline silicon thin films produce polycrystalline layers having undesirably rough polycrystalline silicon film surfaces as well as large grains and grain size variations. In laser crystallization, an amorphous silicon layer is melted by a laser beam, and then the molten silicon is cooled to form a polycrystalline silicon layer. Laser crystallization using pulsed lasers having a 10% variation in laser fluence is common. However, such a variation can cause up to a 1,000% grain size variation in the polycrystalline silicon layer. Thus, the number of grains included in TFT structures manufactured by conventional pulsed laser crystallization varies greatly.

Conventional laser crystallization is practiced on silica, glass or silica buffered substrates. In these systems, the polycrystalline silicon grain size is strongly dependent on laser fluence. This phenomenon is explained by theories variously referred to as the critical laser fluence (see Johnson et al., Materials Research Society Symposium Proceedings vol. 297, page 533, 1993), lateral growth (see Kuriyama et al., Japanese Journal of Applied Physics Letters vol. 33, page 5657, 1994) and super lateral growth (see Im et al., Applied Physics Letters vol. 64, page 2303, 1994). Based on the above theories, silicon grains grow to large lateral dimensions (about 10 times the thickness of the silicon film) in a narrow range of laser fluence. This large lateral grain growth is often accompanied by large surface roughness.

When TFTs are formed in polycrystalline silicon film areas having large crystal grains, the grains are too large to provide a statistically significant number of grains for small TFT feature dimensions. In addition, the large crystal grains in a 100-nm-thick crystallized polycrystalline silicon layer can have a root-mean-square (rms) surface roughness value as large as about 60 nm. Such a large rms surface roughness value cannot support large device bias voltages due to insulator break-

downs.

To avoid the undesirable variations in grain sizes, techniques such as substrate heating are used to improve grain size uniformity in polycrystalline silicon layers. However, substrate heating introduces extra steps in the manufacturing process, thus increasing the process time required to manufacture devices, leading to higher product costs. In view of the above problems, techniques are needed for generating smaller and more uniform polycrystalline silicon grain sizes without increasing manufacturing process time and product costs.

The invention provides in one aspect a buffered substrate comprising a substrate; a buffer layer formed over the substrate; and a silicon layer formed over the buffer layer. The buffer layer has a melting point higher than a threshold temperature of the substrate. After the silicon layer is formed over the buffer layer, it is crystallized using a laser beam.

The substrate is preferably comprised of material selected from silicon, glass, quartz and metal. The buffer layer is preferably comprised of materials such as MgO, MgAl<sub>2</sub>O<sub>4</sub>, Al<sub>2</sub>O<sub>3</sub> and ZrO<sub>2</sub>. The silicon layer may be an amorphous silicon layer and may have a thickness of about 100 nm.

The invention provides in another aspect a method for forming the buffer substrate comprising forming a buffer layer over a substrate. A silicon layer is formed over the buffer layer, and then the silicon layer is crystallized using a laser beam.

The invention is described in detail with reference to the following drawings, wherein like numerals represent like elements:

Fig. 1 is a planar view of a Transmission-Electron-Microscopy (TEM) micrograph of a polycrystalline silicon layer having isotropic and lateral grain growths; and

Figs. 2A-2E show a process of a preferred embodiment.

In laser crystallization processes, the primary cause of large grain size variations is the absence of heterogeneous nucleation by the substrate/liquid-silicon interface. This lack of heterogeneous nucleation results in polycrystalline silicon grains growing to large lateral dimensions (about 10 times the thickness of the silicon film) in a narrow range of laser fluence. This large lateral grain growth is often accompanied by large surface roughness.

In addition, the silicon crystallization process is extremely sensitive to the fluence of the laser used to melt the silicon. This sensitivity to laser fluence is a large factor causing grain size variations and stems from a difference in nucleation density between silicon crystallizing when in contact with unmelted silicon and silicon crystallizing when in contact with an underlying substrate. When the laser fluence is intense enough to "melt-through" portions of the silicon layer, the melted

silicon that contacts the substrate has a different nucleation density from other portions of melted silicon not in contact with the substrate. If the laser fluence is set above a threshold necessary to melt-through all of the silicon layer in an attempt to achieve uniform nucleation density, the substrate is often damaged and causes undesirable effects, such as ablation of the polycrystalline silicon layer.

A preferred embodiment of this invention reduces polycrystalline silicon grain sizes and grain size variations by providing a buffer layer between the substrate and the silicon layer. The buffer layer is formed from materials that can withstand a temperature higher than a threshold temperature of the substrate. If a substrate is heated above its threshold temperature, undesirable effects occur, such as melting the substrate or ablation of films formed over the substrate. Thus, the buffer layer shields the substrate from the above undesirable effects. For example,  $\text{SiO}_2$  substrates have a melting point between about 1610-1723°C. Thus, materials having melting points higher than 1723°C may be used as a buffer layer for  $\text{SiO}_2$  substrates.

In addition to being able to withstand a temperature higher than the threshold temperature of a substrate, the buffer layer also provides for higher silicon nucleation density. When sufficient nuclei exist at the substrate-molten silicon interface, crystallization proceeds to form grains with dimensions approximately equal to that of the thickness of the polycrystalline silicon film. This phenomenon is called isotropic grain growth. The buffer layer promotes isotropic silicon grain growth. The increase of isotropic grain growth avoids large lateral grain growth and reduces lateral grain dimensions to about the thickness of the polycrystalline silicon film.

When molten silicon that contacts the buffer layer is cooled, the increased nucleation density results in smaller silicon grains and greater uniformity in silicon grain sizes. A large number of smaller silicon grains results in a statistically significant number of grains relative to the dimensions of the devices that are formed. The larger number of grains per device leads to more uniform device characteristics and thus more reliable products made from such devices.

A non-exhaustive list of possible materials that meet these requirements for  $\text{SiO}_2$  substrates is shown in the TABLE below.

TABLE

| Material                  | Melting Point °C |
|---------------------------|------------------|
| $\text{MgO}$              | 2852             |
| $\text{MgAl}_2\text{O}_4$ | >2200            |
| $\text{Al}_2\text{O}_3$   | 2980             |
| $\text{ZrO}_2$            | 2700             |

Because these materials have higher melting points

than a  $\text{SiO}_2$  substrate, a buffer layer formed using these materials provides higher resistance to substrate damage caused by laser irradiation.

Limiting substrate damage is particularly important 5 for devices such as bottom gate TFTs. Because the gate electrode is formed on the substrate below active layers of such TFTs, current leakage may occur due to substrate damage. If the gate electrode is formed between the substrate and the buffer layer, the buffer layer thermally 10 protects the substrate while serving as the gate insulator layer of the bottom gate TFT. Thus, the buffer layer improves device performance.

When it is desirable to increase the thermal resistance of the buffer layer, multilayers of high melting point 15 materials may be used. Thus, the buffer layer may be formed of a single layer or of multiple layers depending on the thermal boundary requirements. It may also be advantageous to protect the substrate from thermal damage by extending the amount of time for the melting 20 process or other similar methods.

A polycrystalline silicon layer crystallized by a combination of isotropic and lateral grain growths has regions of low (about unity) and high aspect ratio grains, where the aspect ratio of a grain is a ratio between a 25 width and a height of the grain. Figure 1 shows a TEM micrograph of a sample of such a polycrystalline silicon layer. The grain size variation of polycrystalline silicon films having both isotropic and lateral grain growths is approximately the difference in grain sizes between laterally crystallized grains and isotropically crystallized grains. For example, lateral growth in 100 nm thick silicon films often results in 1 mm grains situated in a matrix of isotropically crystallized grains about 100 nm in size. Thus, the grain size variation is about 10 times.

35 In contrast, the preferred embodiment provides a polycrystalline silicon layer having a grain size variation of less than or equal to about two (2) and an average grain size of less than or equal to about the thickness of the polycrystalline silicon layer.

40 Figures 2A-2E show a process for forming a polycrystalline silicon layer having small and uniform grain sizes. Figure 2A shows a substrate 100 formed from materials such as quartz or glass, for example,  $\text{SiO}_2$ , Corning 7059 or 1731 (Corning 7059 or 1731 are common 45 substrate materials easily obtained from Corning Glass Works, Corning N.Y. 14830). The substrate 100 may also include other structures, such as bottom gate dielectric and gate electrodes for bottom gate devices, for example.

50 Figure 2B shows a buffer layer 102 formed over the substrate 100. The buffer layer 102 may be formed over the substrate 100 by techniques such as physical vapor deposition (i.e. electron beam, sputtering, thermal evaporation, pulsed laser deposition, etc.), chemical vapor deposition (CVD) or solgel processing. Only a thin buffer layer 102 is required, and, in some cases, complete coverage of the surface of the substrate 100 is not necessary. If the buffer layer 102 only partially covers the sur-

face of the substrate 100 and forms islands, an island density should be equal to about the grain density desired for the polycrystalline silicon layer.

In Fig. 2C, an amorphous silicon layer 104 is formed over the buffer layer 102 having a thickness of less than or equal to about 100 nm. Other thicknesses may be used. Amorphous silicon layers with thicknesses of less than or equal to about 100 nm are preferred for pulsed laser crystallization processes because of device related issues. Also, the silicon layer need not be amorphous since the laser beam melts the silicon layer and removes any prior crystalline structure.

The amorphous silicon layer is melted by using a laser beam 106 and then cooled to crystallize the silicon, forming a polycrystalline layer 108 as shown in Figs. 2D and 2E, respectively. The laser beam 106 may be generated by lasers such as a YAG laser or an excimer laser. An excimer laser is often preferred because of the greater process speed due to the wide area of illumination provided by the excimer laser.

Experimental measurements of polycrystalline silicon layers of approximately 100 nm thick formed by conventional laser crystallization indicate that lateral grain growth occurs in a narrow laser fluence range of about  $540 \pm 20 \text{ mJ/cm}^2$  or about 10% of the total possible laser fluence range. This narrow range of laser fluence lies in approximately the center of the laser fluence range required to perform laser crystallization. Thus, to avoid large grain sizes, the laser fluence must be restricted from fluctuating into the narrow laser fluence range. However, because the laser fluence of industrial lasers used for manufacturing devices is difficult to control, the laser fluence output by the industrial lasers must avoid the lateral growth laser fluence range. Thus, the range of laser fluence of industrial lasers available for crystallization is very restricted.

In contrast, the industrial laser fluence control requirements are relaxed when a buffer layer is used. Lateral grain growth is inhibited by the silicon grain nucleation initiated by the buffer layer. In principle, the entire range of laser fluence from melt-through (about 300 mJ/cm<sup>2</sup>) to ablation (about 600 mJ/cm<sup>2</sup>) for 100 nm thick silicon films is available when a buffer layer is present. Thus, with a buffer layer, a much larger laser fluence range is available.

The process shown in Figs. 2A-2E forms a polycrystalline silicon layer 108 having an average grain size variation of less than or equal to about two (2), as compared to a grain size variation of 10 for conventional techniques. Thus, the buffer layer 102 reduces grain size variations by at least a factor of five (5).

The uniformity of the grain sizes of the polycrystalline layer 108 is also greatly improved, resulting in greater uniformity of device characteristics formed in the polycrystalline layer 108. Devices such as TFTs, capacitors and resistors are more reliable, leading to superior products.

Further, for polycrystalline silicon layers having a

thickness of about 100 nm, an rms surface roughness value of the polycrystalline silicon layer 108 is about 6 nm or less. This is an order of magnitude improvement over the rms surface roughness value of 60 nm produced by conventional laser crystallization techniques in the lateral growth regime.

The principles described herein would also apply to pulsed laser crystallization of microcrystalline Si, Ge or SiGe alloys.

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## Claims

1. A buffered substrate, comprising:

a substrate (100);  
a buffer layer (102) formed over the substrate (100), the buffer layer (102) having a melting point higher than a threshold temperature of the substrate (100); and  
a silicon layer (104) formed over the buffer layer (102), wherein the silicon layer (104) is crystallizable using a laser beam after being formed over the buffer layer (102).

2. The buffered substrate of claim 1, wherein the substrate (100) comprises at least one of silicon, glass, quartz and metal.

3. The buffered substrate of either of claims 1 or 2, wherein the buffer layer (102) forms islands over the substrate (100).

4. The buffered substrate of any of claims 1 to 3, wherein the buffer layer (102) comprises at least one of MgO, MgAl<sub>2</sub>O<sub>4</sub>, Al<sub>2</sub>O<sub>3</sub> and ZrO<sub>2</sub>.

5. The buffered substrate of any of claims 1 to 4, wherein the silicon layer (106) is an amorphous silicon layer, the amorphous silicon layer being crystallizable to form a polycrystalline silicon layer.

6. The buffered substrate of claim 5, wherein the thickness of the amorphous silicon layer is less than or equal to about 100 nm, and the grain size variation of the polycrystalline silicon layer is less than or equal to about 2.

7. The buffered substrate of claim 5, wherein the average grain size of the polycrystalline silicon layer is less than about the thickness of the polycrystalline silicon layer.

8. The buffered substrate of claim 5, wherein a root-mean-square roughness of the polycrystalline silicon layer is less than or equal to about 6 nm.

9. A method for forming a buffered substrate, compris-

ing:

forming a buffer layer (102) over a substrate (100), the buffer layer (102) having a melting point higher than a threshold temperature of the substrate (100);  
forming a silicon layer (104) over the buffer layer (102); and then  
crystallizing the silicon layer using (104) a laser beam.

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10. The method of claim 9, wherein the laser beam is one of an excimer laser beam and a YAG laser beam.

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FIG. 1

FIG.2A



FIG.2B

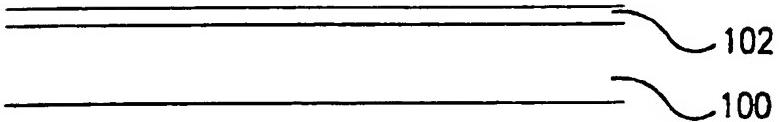


FIG.2C

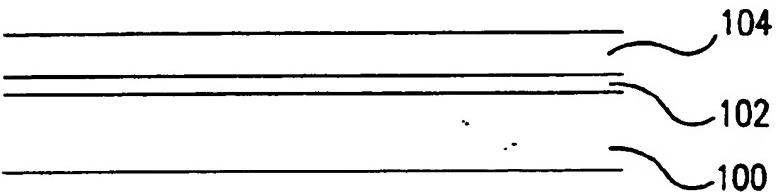


FIG.2D

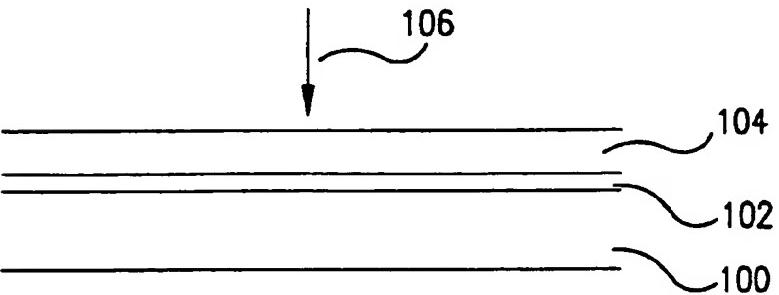
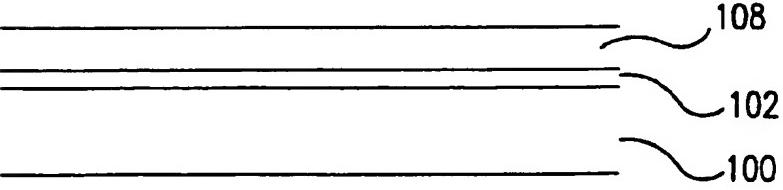


FIG.2E







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(11)

EP 0 810 638 A3

(12)

## EUROPEAN PATENT APPLICATION

(88) Date of publication A3  
03.02.1999 Bulletin 1999/05

(51) Int Cl. 6: H01L 21/20, H01L 21/316

(43) Date of publication A2  
03.12.1997 Bulletin 1997/49

(21) Application number 97303455.6

(22) Date of filing 21.05.1997

(84) Designated Contracting States  
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Santa Cruz, California 95060 (US)

(71) Applicant: XEROX CORPORATION  
Rochester, New York 14644 (US)

• Johnson, Richard I.  
Menlo Park, California 94025 (US)

(72) Inventors:

• Anderson, Greg B.  
Woodside, California 94062 (US)

- Fork, David K.  
Palo Alto, California 94306 (US)
- Boyce, James B.  
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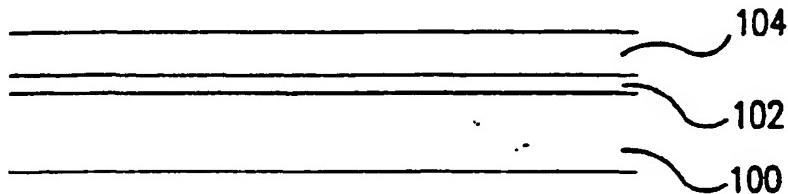
(74) Representative: Pike, Christopher Gerard et al  
Rank Xerox Ltd.,  
Patent Department,  
Parkway  
Marlow, Buckinghamshire SL7 1YL (GB)

(54) Buffered substrate for semiconductor devices

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FIG.2C





European Patent  
Office

## EUROPEAN SEARCH REPORT

Application Number  
EP 97 30 3455

| DOCUMENTS CONSIDERED TO BE RELEVANT  |  |                   |   |                 |                                  |          |           |                  |         |
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| Category   | Citation of document with indication, where appropriate, of relevant passages  | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int.Cl.6)    |                 |                                  |          |           |                  |         |
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| <p>The present search report has been drawn up for all claims</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 33%;">Place of search</td> <td style="width: 33%;">Date of completion of the search</td> <td style="width: 34%;">Examiner</td> </tr> <tr> <td>THE HAGUE</td> <td>26 November 1998</td> <td>Köpf, C</td> </tr> </table> <p>CATEGORY OF CITED DOCUMENTS</p> <p>X : particularly relevant if taken alone<br/>     Y : particularly relevant if combined with another document of the same category<br/>     A : technological background<br/>     O : non-written disclosure<br/>     P : intermediate document</p> <p>T : theory or principle underlying the invention<br/>     E : earlier patent document, but published on, or after the filing date<br/>     D : document cited in the application<br/>     L : document cited for other reasons<br/>     &amp; : member of the same patent family, corresponding document</p> |  |                   |   | Place of search | Date of completion of the search | Examiner | THE HAGUE | 26 November 1998 | Köpf, C |
| Place of search  | Date of completion of the search   | Examiner          |   |                 |                                  |          |           |                  |         |
| THE HAGUE  | 26 November 1998   | Köpf, C           |   |                 |                                  |          |           |                  |         |

ANNEX TO THE EUROPEAN SEARCH REPORT  
ON EUROPEAN PATENT APPLICATION NO.

EP 97 30 3455

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.  
The members are as contained in the European Patent Office EDP file on  
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26-11-1998

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